AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus for variably scaling video picture signals comprising:

a first circuit configured to generate one or more data signals vertically scaled to a first value in response to (i) said video picture signals and (ii) one or more first control signals;

a second circuit configured to generate one or more output signals horizontally scaled to a second value in response to (i) said one or more data signals and (ii) said one or more first control signals, wherein said first value and said second value are independently selectable; and

an address generator circuit configured to generate said one or more first control signals, wherein said address ~~generated~~ generator comprises a finite state machine configured to allow multiple luma and multiple chroma picture requests to follow in sequence.

2. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said first circuit comprises (i) a luma circuit configured to generate a luma component of said data signals and (ii) a chroma circuit configured to generate one or more chroma components of said data signals.

3. (ORIGINAL) The apparatus according to claim 1, wherein said second circuit is further configured to decimate and interpolate said data signals.

4. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is programmable to scale said output signals to one or more display modes.

5. (ORIGINAL) The apparatus according to claim 4, wherein said apparatus is configured to automatically reset a starting address of a display line when an end of said display line is not displayed.

6. (PREVIOUSLY PRESENTED) The apparatus according to claim 4, wherein said one or more output signals are scalable to any value in a range of 0.25 times to 4.0 times said video picture signals.

7. (PREVIOUSLY PRESENTED) The apparatus according to claim 2, wherein said luma circuit comprises:

a first memory circuit configured to buffer a luma component of said video picture signals;

a first filter circuit coupled to said first memory circuit and configured to generate said luma component of said data signals; and

a second memory circuit coupled to said first filter circuit and configured to buffer said luma component of said data signals.

8. (PREVIOUSLY PRESENTED) The apparatus according to claim 7, wherein said chroma circuit comprises:

a third memory circuit configured to buffer one or more chroma components of said video picture signals;

a second filter circuit coupled to said third memory circuit and configured to generate said one or more chroma components of said data signals; and

a fourth memory circuit coupled to said second filter circuit and configured to buffer said one or more chroma components of said data signals.

9. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said generator circuit is configured to generate said control signals in response to one or more second control signals from a microcontroller circuit.

10. (ORIGINAL) The apparatus according to claim 9, wherein said apparatus comprises a single-chip MPEG-2 decoder.

11. (PREVIOUSLY PRESENTED) The apparatus according to claim 7, wherein said first filter circuit further comprises one or more accumulator circuits configured to define a number of said video picture signals to be buffered in said first memory circuit in response to said one or more first control signals.

12. (PREVIOUSLY PRESENTED) The apparatus according to claim 8, wherein said second filter circuit further comprises one or more accumulator circuits configured to define a number of said video picture signals to be buffered in said third memory circuit in response to said one or more first control signals.

13. (ORIGINAL) The apparatus according to claim 1, wherein said second circuit controls an output rate of said data signals from said first circuit in response to said first value and said second value.

14. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said second circuit comprises one or more accumulator circuits configured to select one or more of said data signals in response to said one or more first control signals.

15. (PREVIOUSLY PRESENTED) An apparatus for variably scaling video picture signals comprising:

means for generating one or more data signals vertically scaled to a first value in response to (i) said video picture signals and (ii) one or more control signals;

means for generating one or more output signals horizontally scaled to a second value in response to (i) said one or more data signals and (ii) said one or more control signals, wherein said first value and said second value are independently selectable; and

means for generating said one or more control signals configured to provide a number of states configured to allow multiple luma and chroma picture requests to follow in sequence.

16. (PREVIOUSLY PRESENTED) A method for variably scaling video picture signals comprising the steps of:

(A) generating one or more data signals vertically scaled to a first value in response to (i) said video picture signals and (ii) one or more control signals;

(B) generating one or more output signals horizontally scaled to a second value in response to (i) said one or more data signals and (ii) said one or more control signals, wherein said first value and said second value are independently selectable; and

(C) generating said one or more control signals in response to a number of states configured to allow multiple luma and chroma picture requests to follow in sequence.

17. (ORIGINAL) The method according to claim 16, wherein step B further comprises the steps of:

decimating said data signals; and

interpolating said data signals.

18. (PREVIOUSLY PRESENTED) The method according to claim 16, wherein step B further comprises the step of:

controlling an output rate of said data signals in response to said first value and said second value.

19. (ORIGINAL) The method according to claim 16, wherein said method further comprises the step of:

programmably scaling said output signals to one or more display modes.

20. (PREVIOUSLY PRESENTED) The method according to claim 19, wherein said step of programmably scaling said output signals further comprises the step of:

automatically resetting a display line address when some of a picture is not displayed.

21. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said finite state machine comprises an idle after chroma state configured to move to any of (i) a luma state, (ii) a BTMP after luma state, (iii) an SPU/VBI state, (iv) an idle after luma state, and (v) a chroma state.

22. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said finite state machine comprises an idle after luma state configured to move to any of (i) a chroma state, (ii) a BTMP after chroma state, (iii) an SPU/VBI state, (iv) a luma state and (v) an idle after chroma state.

23. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said finite state machine provides (i) an idle after chroma state configured to move to a chroma state in response to a first predetermined condition and (ii) an idle after luma state configured to move to a luma state in response to a second predetermined condition.